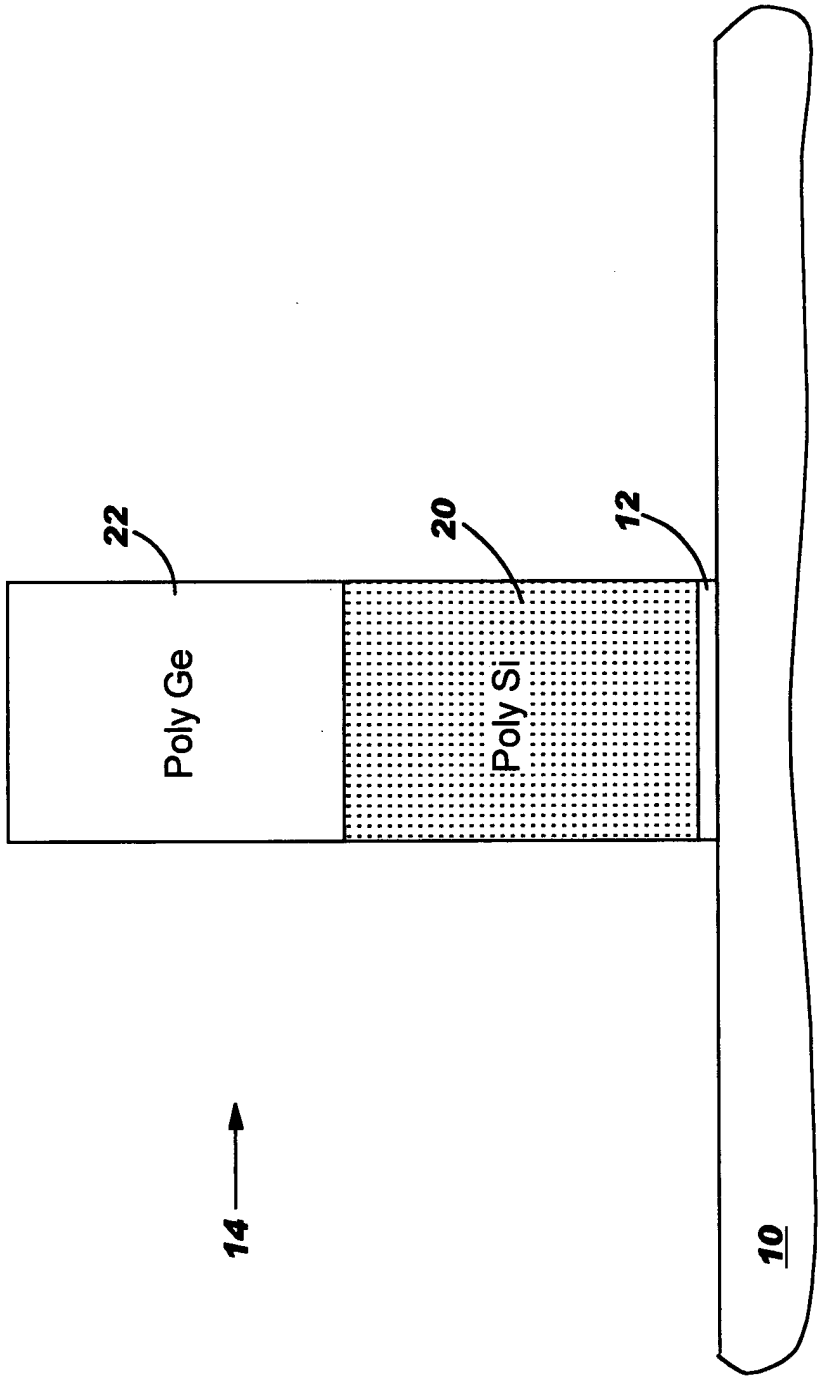
FIG. 1



- STI, N and P Well,
- gate dielectric formation (plasma nitrided thermal oxidation or deposited oxynitride or nitride)
- Intrinsic polySi (~150nm) and intrinsic polyGe (~150nm) deposition
- Poly Si and PolyGe stack etch

FIG. 2

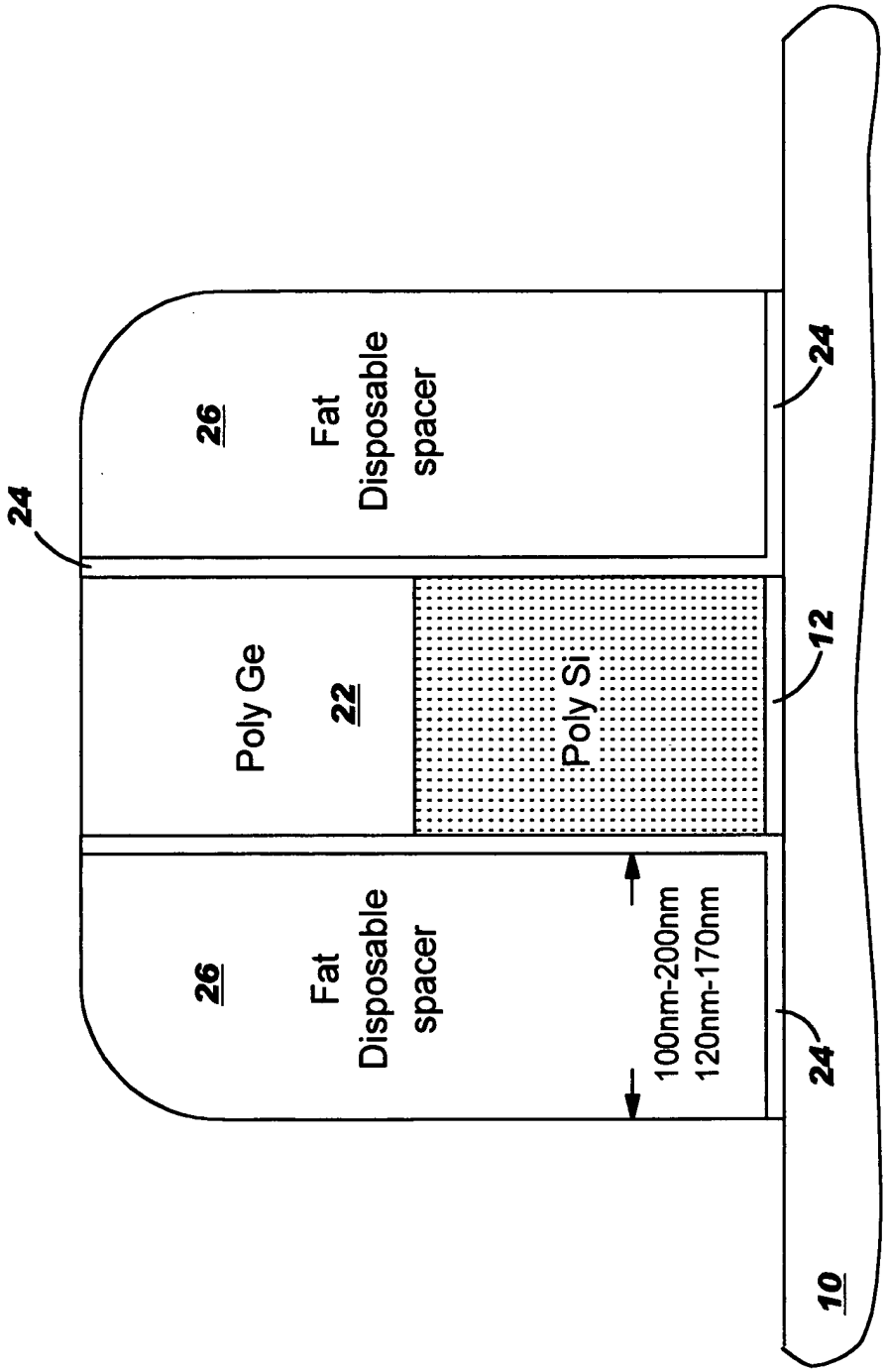

26
Fat
Disposable
spacer
24
Poly Ge
22
Poly Si
12
26
Fat
Disposable
spacer
100nm-200nm
120nm-170nm
24
10
Fat Spacer formation
– Oxide/nitride liner deposition
– Conformal CVD or plasma CVD SiO2 deposition
– RIE directional etching of SiO2

FIG. 3

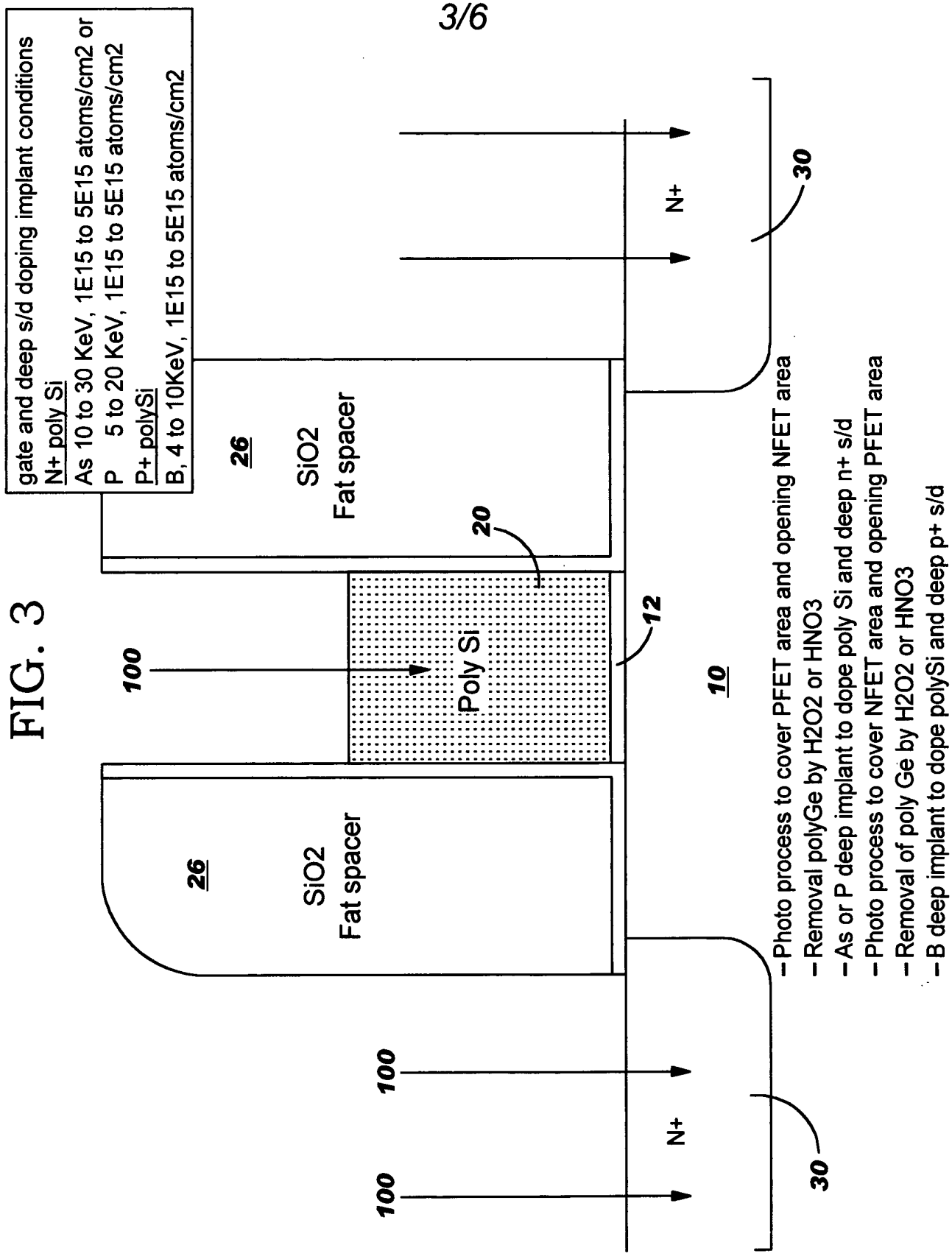

gate and deep s/d doping implant conditions
N+ poly Si
As 10 to 30 KeV, 1E15 to 5E15 atoms/cm2 or
P 5 to 20 KeV, 1E15 to 5E15 atoms/cm2
P+ polySi
B, 4 to 10KeV, 1E15 to 5E15 atoms/cm2
26
SiO2
Fat spacer
20
100
Poly Si
12
10
N+
30
– Photo process to cover PFET area and opening NFET area
– Removal polyGe by H2O2 or HNO3
– As or P deep implant to dope poly Si and deep n+ s/d
– Photo process to cover NFET area and opening PFET area
– Removal of poly Ge by H2O2 or HNO3
– B deep implant to dope polySi and deep p+ s/d

FIG. 4

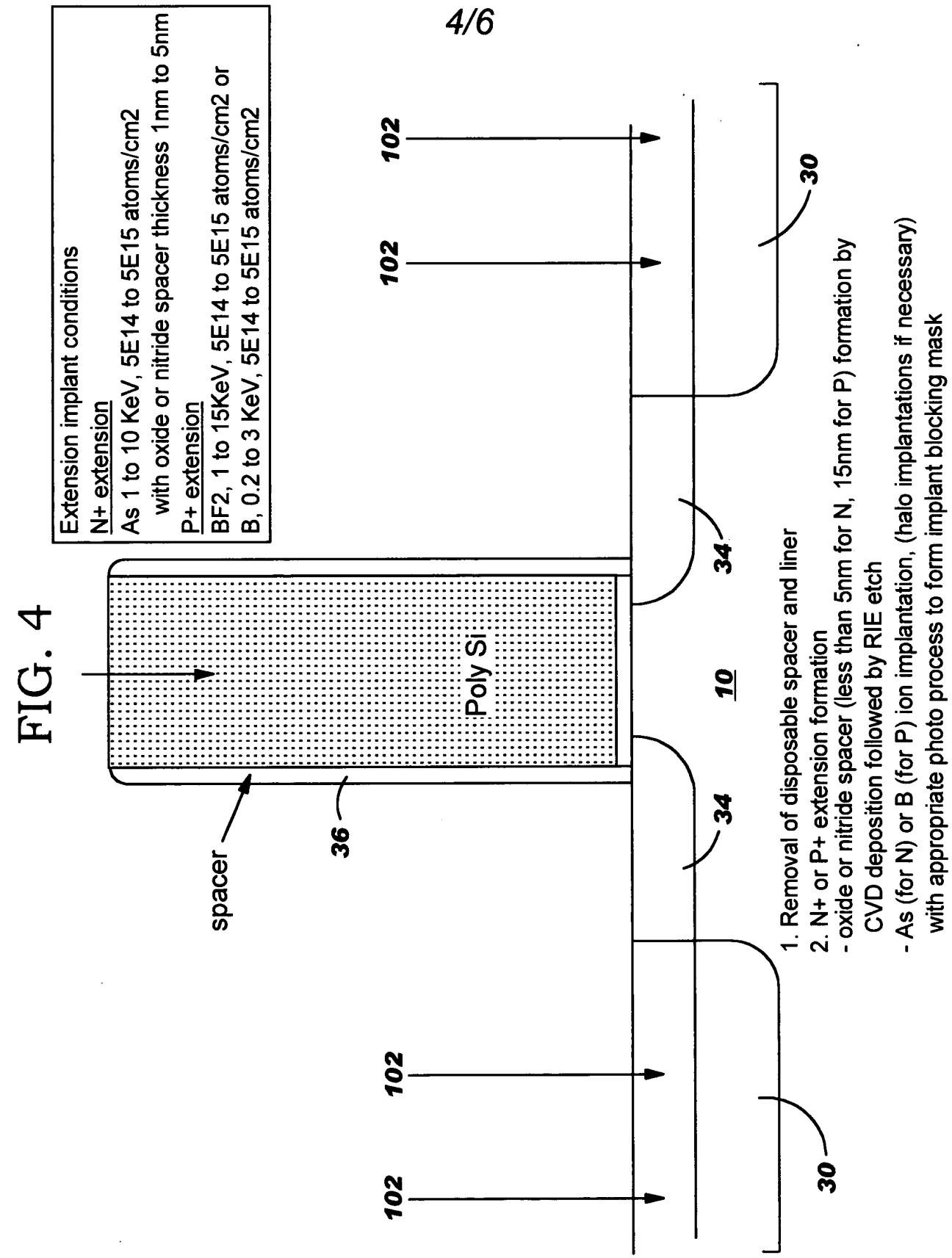
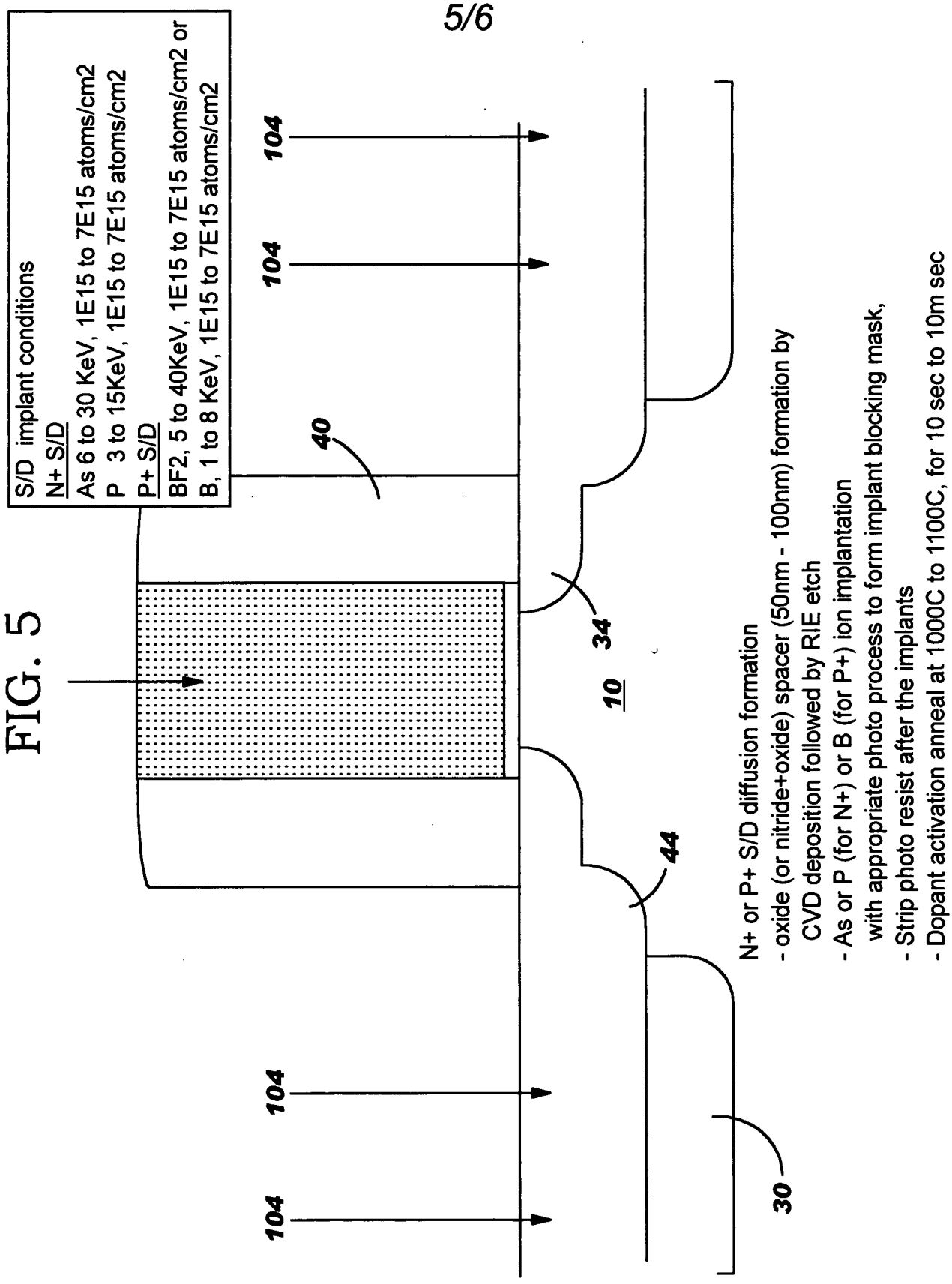

Extension implant conditions
N+ extension
As 1 to 10 KeV, 5E14 to 5E15 atoms/cm2
with oxide or nitride spacer thickness 1nm to 5nm
P+ extension
BF2, 1 to 15KeV, 5E14 to 5E15 atoms/cm2 or
B, 0.2 to 3 KeV, 5E14 to 5E15 atoms/cm2
102
102
102
102
Poly Si
spacer
36
34
34
10
30
30
1. Removal of disposable spacer and liner
2. N+ or P+ extension formation
- oxide or nitride spacer (less than 5nm for N, 15nm for P) formation by CVD deposition followed by RIE etch
- As (for N) or B (for P) ion implantation, (halo implantations if necessary) with appropriate photo process to form implant blocking mask

FIG. 5


S/D implant conditions
N+ S/D
As 6 to 30 KeV, 1E15 to 7E15 atoms/cm2
P 3 to 15KeV, 1E15 to 7E15 atoms/cm2
P+ S/D
BF2, 5 to 40KeV, 1E15 to 7E15 atoms/cm2 or
B, 1 to 8 KeV, 1E15 to 7E15 atoms/cm2
104
104
104
104
40
34
10
44
30
N+ or P+ S/D diffusion formation
- oxide (or nitride+oxide) spacer (50nm - 100nm) formation by
CVD deposition followed by RIE etch
- As or P (for N+) or B (for P+) ion implantation
with appropriate photo process to form implant blocking mask,
- Strip photo resist after the implants
- Dopant activation anneal at 1000C to 1100C, for 10 sec to 10m sec

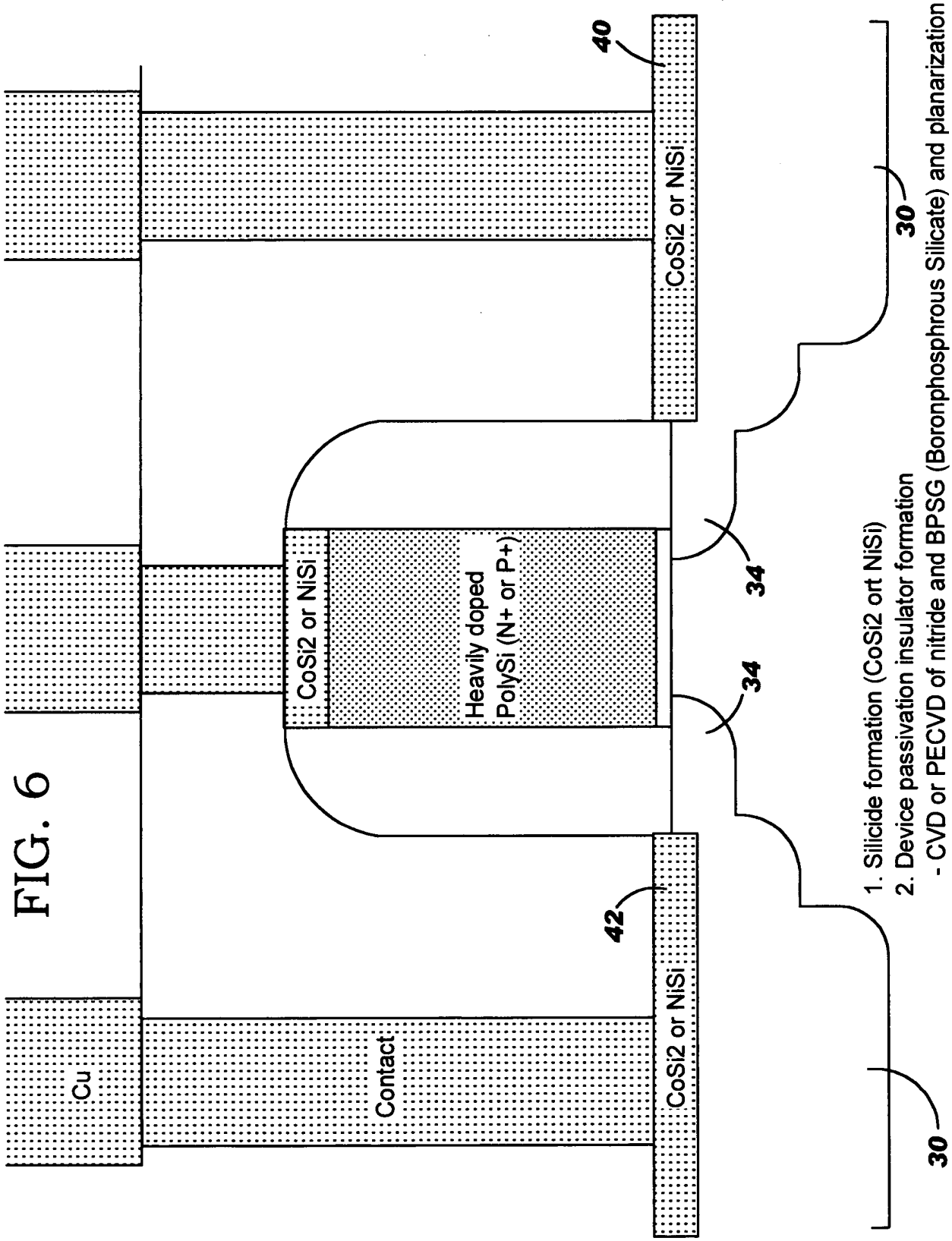

40
CoSi2 or NiSi
30
34
CoSi2 or NiSi
Heavily doped
PolySi (N+ or P+)
34
42
Cu
Contact
CoSi2 or NiSi
30
1. Silicide formation (CoSi2 ort NiSi)
2. Device passivation insulator formation
- CVD or PECVD of nitride and BPSG (Boronphosphrous Silicate) and planarization
3. Contact (W stud) and metal (Cu or Al) wiring formatoin

FIG. 6